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P-type gate electrode. For the reasons stated below, amended claim 1, dependent claims 2-73 and newly added claims 74-89 are patentably distinct over the prior art of record.

Claims 1, 2, 4, 11, 15, 16, 43 and 54 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,554,873 to Erdeljac et al. ("Erdeljac") in view of U.S. Patent No. 4,559,694 to Yoh et al. ("Yoh"). Erdeljac was cited as disclosing a complementary MOS semiconductor device in Fig. 11 having an N-channel MOS transistor 44, a P-channel MOS transistor 50 and a resistor. Yoh was cited as disclosing a complementary MOS semiconductor device in Figs. 59 and 60 having an N-channel MOS transistor Q4 with a P-type gate electrode and a P-channel MOS transistor Q1 with a P-type gate electrode.

The basis of the Examiner's obviousness rejection is the purported obviousness of combining Erdeljac with Yoh so as to form gate electrodes of the P-channel MOS transistor 50 and the N-channel MOS transistor 44 of Erdeljac with the P-type polycrystalline silicon disclosed by Yoh instead of the N-type polycrystalline silicon used in Erdeljac in order to obtain transistors having low threshold voltages that can operate at low voltage and consume low power.

As pointed out in the introductory portion of applicants' specification, conventional CMOS semiconductor devices comprise an NMOS transistor with a gate electrode

formed of N+ type polysilicon on a P-type semiconductor substrate and a PMOS transistor 212 with a gate electrode formed of N+ type polysilicon in an N-well region of the P-type substrate. A resistor may also be included in the CMOS device.

A typical enhancement type NMOS has a threshold voltage of approximately 0.7V and has a gate electrode formed of N+ polycrystalline silicon. Such a transistor is a surface channel device with a channel region formed on a surface of the substrate. On the other hand, an enhancement type PMOS with a typical threshold voltage of about -0.7V is a buried channel device having a channel buried beneath the surface of the substrate.

In a buried channel enhancement mode PMOS transistor, when the threshold voltage is set to about -0.5V for low voltage operation, the sub-threshold characteristics deteriorate and the leak current increases. As a result, consumption current of the semiconductor device increases, which is incompatible with use of the semiconductor device in a portable electronic apparatus.

In order to overcome the above-described problem and achieve low voltage operation and low consumption current, the conductivity type of an NMOS gate electrode is set as N-type and the conductivity type of a PMOS gate electrode is set as

P-type. In this case, both the enhancement mode NMOS and the enhancement mode PMOS are surface channel MOS transistors. In such devices, lowering of the threshold voltage does not lead to the deterioration in sub-threshold characteristics.

However, the manufacture of complementary surface channel devices increases the number of processing steps and the manufacturing cost compared to a typical CMOS device in which the gate electrode is an N+ polycrystalline silicon monopole, since the gate polarities are separately formed for the NMOS and PMOS devices.

The present invention overcomes this drawback by providing a structure of a CMOS device in which the goals of low cost, short manufacturing time, low voltage operation and low power consumption can be achieved.

In accordance with amended independent claim 1, the inventive CMOS semiconductor device comprises a semiconductor substrate, a CMOS transistor pair comprised of an N-channel MOS transistor formed in the semiconductor substrate and a P-channel MOS transistor formed in the semiconductor substrate, the N-channel MOS transistor and P-channel MOS transistor forming a CMOS transistor pair, and a resistor formed in the semiconductor substrate, wherein a conductivity type of the gate electrodes of the N-channel MOS transistor and the P-channel MOS transistor is P-type.

In accordance with newly added independent claim 88 and dependent claim 87, the inventive CMOS semiconductor device is for a voltage regulator, the N-channel MOS transistor is used in a reference voltage generating circuit of the voltage regulator and the P-channel MOS transistor is used as an output element of the voltage regulator. Newly added independent claim 89 recites that the CMOS semiconductor device is for a voltage regulator, and that the resistor is used in a voltage divider of the regulator.

Since the gate electrode of the P-channel MOS transistor is formed of P+ polycrystalline silicon, an enhancement mode transistor is a surface channel device. Thus, the setting of a threshold voltage to a level in the range of -0.5V does not lead to deterioration of the sub-threshold characteristics. Accordingly, low voltage operation and low power consumption are possible.

On the other hand, the N-channel MOS transistor is a buried channel device in the enhancement mode. However, since arsenic can be used as a donor impurity for threshold control (claim 86), the channel is an extremely shallow buried channel. Thus, deterioration in sub-threshold characteristics and increase in leak current are greatly reduced in comparison with an enhancement mode P-channel MOS transistor having a gate electrode formed of N+ polycrystalline silicon and a deep

buried channel resulting from the use of boron as an acceptor impurity.

No corresponding structure is disclosed or suggested by the prior art of record.

The CMOS circuit of Erdeljac includes an NMOS transistor 44, a PMOS transistor 50 and a resistor. However, the NMOS and PMOS transistors do not have P-type gate electrodes. Figs. 59 and 60 of Yoh include an NMOS transistor Q4 having a P-type gate electrode and a PMOS transistor Q1 having a P-type gate electrode. However, transistors Q1 and Q4 of Yoh are not a complementary pair. Applicants respectfully submit that the Examiner's reliance on Yoh as suggesting modification of Erdeljac in the claimed manner is misplaced.

Neither Erdeljac nor Yoh discloses or suggests a complementary transistor pair each having a P-type polycrystalline silicon gate electrode. Thus the combined teachings of the cited references fail to teach the subject matter recited by amended independent claim 1 or the newly added independent claims.

When considered as a whole, neither of the cited references would have explicitly suggested the modification urged by the Examiner. Nor do the references suggest the desirability of such modification. There is nothing in either

of the references that would have suggested modifying a complementary MOS device to provide an NMOS transistor and a PMOS transistor with P-type gate electrodes as recited by amended independent claim 1. Nor do the references disclose or suggest use of the NMOS transistor and the PMOS transistor in the reference voltage generating circuit and as an output device of the voltage regulator as recited by claims 87 and 88.

A claim rejection based upon obviousness under 35 U.S.C. §103(a) must be supported by an evidentiary basis establishing the obviousness of each limitation of a rejected claim. This burden may be satisfied by citation of a single reference which requires an obvious modification to replicate the claimed invention, or by a combination of references which satisfies all claim limitations, along with a cogent line of reasoning consistent with the cited reference(s) and demonstrating why such modification or combination would have been obvious to the ordinarily skilled practitioner. Mere speculation or conclusory allegations are inadequate to meet this burden. Any modification or combination that purportedly renders an invention unpatentable must be suggested by some teaching or motivation found in the prior art. Stated otherwise, the desirability of any modification or combination urged by the Examiner must be disclosed, suggested, or

motivated by the prior art. See, e.g., Symbol Technologies, Inc. v. Opticon, Inc., 935 F.2d 982, 989, 18 USPQ2d 1885 (Fed. Cir. 1991).

In order to set forth a prima facie case of obviousness, the Examiner must demonstrate not only that all limitations of a rejected claim exist in the prior art, but that a suggestion to combine elements found in a variety of references is also found in those references. This burden cannot be met by citing references that lack such motivation. "Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. Under section 103, teachings of references can be combined only if there is some suggestion or incentive to do so." In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992). Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious 'modification' of the prior art. The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. Id.

In the instant case, the Examiner has not met his burden of establishing a prima facie case of obviousness as discussed above. There is nothing in either Erdeljac or Yoh

that would expressly or impliedly teach or suggest the combination urged by the Examiner. Erdeljac and Yoh fail to suggest any motivation for, or desirability of, the changes espoused by the Examiner.

Here, the Examiner relied upon hindsight to arrive at the determination of obviousness. It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art to replicate the claimed invention. Id.

As pointed out by the Federal Circuit in In re Oeticker, 24 USPQ2D 1443, 1444 (Fed. Cir. 1992), "[i]f examination at the initial stage does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of the patent (citing In re Grabiak, 769, F.2d 729, 733, 226 USPQ 870, 873 (Fed. Cir. 1985)).

The Federal Circuit has therefore made it clear that the prior art must show an incentive to combine the teachings of the prior art in order to support an obviousness rejection. Absent such an incentive, a *prima facie* rejection of obviousness cannot be made.

The sole motivation for using P-type gate electrodes in both the N-channel MOS transistor and the P-channel MOS transistor of a CMOS transistor pair is found in applicants' disclosure. It is impermissible to use applicants' disclosure

as a roadmap to piece together isolated elements found in the prior art in the manner done by the Examiner.

As discussed by applicants, a homopolar gate CMOS has an NMOS and PMOS with gate electrodes of different polarities which must be separately formed. Thus, the homopolar device requires a larger number of processing steps and is more expensive than a conventional CMOS device -- in which the gate electrode is an N+ polycrystalline silicon monopole.

The present invention requires that the NMOS and PMOS transistors of a CMOS transistor pair have P-type gate electrodes and uses the respective CMOS transistors in a novel and unique manner in order to take advantage of the benefits of each device. In one example, the PMOS is a surface channel enhancement mode device and the NMOS is an enhancement mode device having a shallow buried channel formed using arsenic as a donor impurity. Since the channel is extremely shallow, only slight deterioration in sub-threshold characteristics and increase in leak current occur.

Since the gate electrode of the PMOS is formed of P type polycrystalline silicon, an enhancement mode PMOS transistor according to the present invention is a surface channel device. Thus, the setting of a threshold voltage to a level in the range of -0.5V does not lead to deterioration of

the sub-threshold characteristics. Accordingly, low voltage operation and low power consumption are possible.

Accordingly, a voltage regulator employing the inventive CMOS device using the NMOS as part of the reference voltage generating circuit and the PMOS as an output device does not suffer from the drawbacks associated with the conventional device described above.

The cited references contain no motivation for modifying the gate electrodes of the CMOS transistor pair of Erdeljac in the manner suggested by the Examiner.

Erdeljac discloses a semiconductor device having a p-type polysilicon resistor 56 with a moderate sheet resistance and low temperature coefficient of resistance formed by a double-level polysilicon process. The process also produces NMOS and PMOS transistors 44, 50, a capacitor having upper and lower N-type polysilicon capacitor plates 36, 26, an N-type polysilicon resistor 32 having a high sheet resistance, and an N-type resistor 34 having a low sheet resistance. The P-type doping used to form source/drain regions 48 of the PMOS transistor 50 counterdopes N-type second level polysilicon to form the P-type polysilicon resistor 56 without effecting capacitor plates 36, 26 or the N-type resistors 32, 34.

Erdeljac does not suggest forming the gate electrodes of the NMOS and PMOS transistors of P-type polycrystalline silicon as recited by amended independent claim 1 and newly added independent claims 88 and 89.

Yoh does not suggest modifying Erdeljac to form gate electrodes of the complementary NMOS and PMOS transistors of P-type polycrystalline silicon. Yoh discloses a method for manufacturing a reference voltage generating circuit which detects a voltage corresponding to an energy gap of a semiconductor device and generates the detected voltage as a reference voltage. The reference voltage is generated by detecting a difference in threshold voltages of first and second IGFETs. Gate electrodes of the first and second IGFETs are formed on gate insulating films which are formed on different surface areas of an identical semiconductor substrate under substantially the same conditions. The gate electrodes of the first and second IGFETs are respectively formed of two semiconductors which are selected from among a semiconductor of a first conductivity type, a semiconductor of a second conductivity type and an intrinsic semiconductor formed of an identical semiconductor material, but which have Fermi energy levels of values different from each other. Yoh does not disclose an NMOS transistor and PMOS transistor arranged in a CMOS pair as recited by amended independent

claim 1 or newly added independent claims 88 and 89. Nor does Yoh suggest modifying Erdeljac to form the PMOS transistor as a surface channel device and the NMOS transistor as a buried channel device using arsenic as an impurity as recited by various dependent claims.

Although Yoh discloses IGFETs having gate electrodes with the same conductivity type, Yoh does not disclose or suggest that such IGFETs are formed together as complementary MOS transistors.

Accordingly, applicants respectfully submit that amended independent claim 1, dependent claims 2-73, and newly added claims 74-93 patentably distinguish over the prior art of record and that the rejections under 35 U.S.C. §103(a) should be withdrawn.

In view of the foregoing amendments and discussion, the application is believed to be in condition for allowance.

Accordingly, favorable reconsideration and allowance of the claims are most respectfully requested.

Respectfully submitted,

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Debra Buonincontri
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July 30, 2003
Date

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Paragraph beginning at line 3 of page 91 has been amended as follows:

The formation of the P+resistor 116 and the N+resistor 117 is attained by simultaneously doping the impurity into the polycrystalline silicon in the formation of a source and a drain of the NMOS and PMOS. In this case, as to the P+resistor 116, boron or BF_2 is used as the impurity with a concentration of approximately 1 x 10^{19} atoms/cm^3 or more, a sheet resistance value of approximately several hundred [of] Ω/square to 1 kΩ/square, and a temperature coefficient of approximately several hundred [of] ppm/°C to 1000 ppm/°C. As to the N+resistor 117, phosphorous or arsenic is used as the impurity with a concentration of approximately 1 x 10^{19} atoms/cm^3 or more, a sheet resistance value of approximately one hundred [of] Ω/square to several hundred [of] Ω/square, and a temperature coefficient of approximately several hundred [of] ppm/°C to 1000 ppm/°C. Further, Fig. 2 shows both the N+resistor <u>117</u> [118] and the P+resistor <u>116</u> [117]. However, one of these resistors may constitute the semiconductor device for the purpose of reducing the number of steps and cost in consideration of the characteristics

required for the semiconductor device and characteristics of the resistors.

Paragraph beginning at line 6 of page 136 has been amended as follows:

Next, as shown in Fig. 55 [30], the thin film polycrystalline silicon 136 is patterned by the photolithography [photolothography] method and etching to form a resistor.

IN THE CLAIMS:

Claim 1 has been amended as follows:

1. (Twice Amended) A complementary MOS semiconductor device [for a voltage regulator], comprising: a semiconductor substrate; a CMOS transistor pair comprised of an N-channel MOS transistor formed in the semiconductor substrate and [used in a reference voltage generating circuit of the voltage regulator;] a P-channel MOS transistor formed in the semiconductor substrate, the N-channel MOS transistor and the P-channel MOS transistor forming a complementary transistor pair [and used as an output element of the voltage regulator]; and a resistor formed ~~in~~ on the semiconductor substrate; wherein a conductivity type of a gate electrode of the N-channel MOS transistor is P-type, and a conductivity

type of a gate electrode of the P-channel MOS transistor is P-type.